AzureWave Technologies, Inc.

AW-XM455MA

IEEE 802.11 2x2 Wi-Fi 6 MIMO Wireless LAN + Bluetooth 5.1 Combo M.2 2230 Module

Datasheet

Rev. A

DF

For Standard

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Features

WLAN

- Support 2x2 802.11 a/b/g/n/ac/ax
- Dual bands: 2.4 GHz and 5 GHz
- Support 20/40/80 MHz channel Bandwidths.
- 5GHz PHY data rates up to 1.2 Gbps
- 2.4 GHz PHY data rates up to 458 Mbps
- Uplink and downlink OFDMA and MU-MIMO
- Instantaneous 0-DFS

Bluetooth

- Bluetooth 5.1
- Bluetooth class 2
- PCM interface for voice applications
- 2Mbit/s LE
- Long range
- LTE/MWS coexistence
- 2 x wide band speech (WBS) calls
- Security: AES

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Revision History

Document NO: R2-2455MA-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2021/05/17	DCN020299	● Draft version	Renton Tao	N.C Chen

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AzureWave Technologies, Inc.

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1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the Wi-Fi 6 2x2 and BT combo module – **AW-XM455MA.** With High Efficiency Wireless (HEW) and backward compatible with 802.11ac technologies integrated into a module, AW-XM455MA provides the best and most convenient SMT process. The module is targeted to mobile devices including**,** Tablet PC, Portable Media Players (PMPs), Portable Navigation Devices (PNDs), Personal Digital Assistants (PDAs), Tracking Devices, Gaming Devices which need convenient SMT process, low power consumption.

By using AW-XM455MA, the customers can easily integrate the Wi-Fi and BT by a combo module with the benefits of **high design flexibility, high success rate on SMT process, short development cycle, and quick time-to-market.**

Compliance with the IEEE 802.11a/b/g/n/ac/ax standard, the AW-XM455MA uses **DSSS**, **OFDM**, **DBPSK**, **DQPSK**, **CCK** and **QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-XM455MA.

The AW-XM455MA supports standard interface **PCIe for WLAN** interface connection. High-Speed **UART for BT** interface connection. AW-XM455MA is suitable for multiple mobile processors for different applications. With the combo functions and the good performance, the AW-XM455MA is the best solution for the consumer electronics and the tablet PC.

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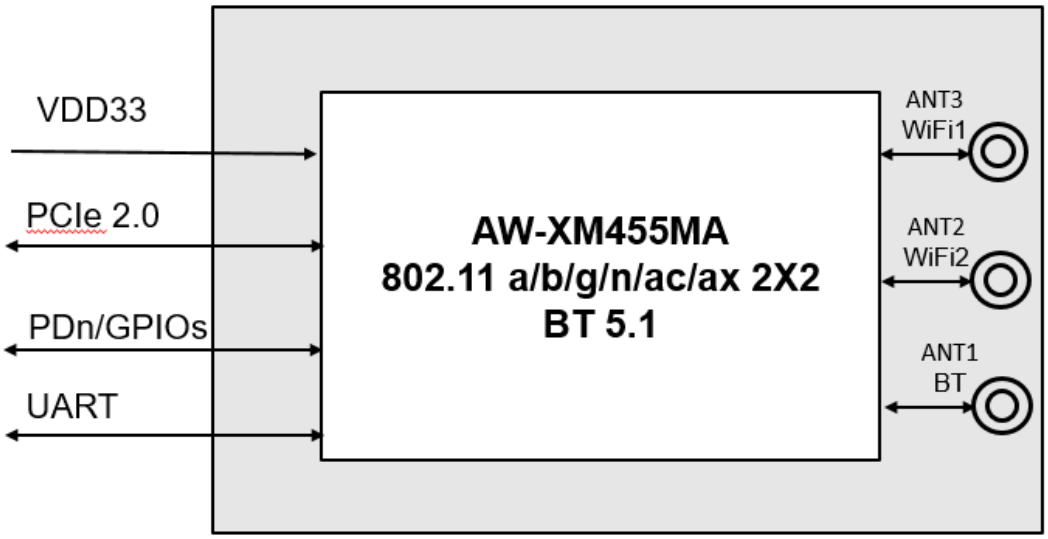
1.2 Block Diagram

A simplified block diagram of the AW-XM455MA module is depicted in the figure below.



AW-XM455MA Block Diagram

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1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11 2X2 WiFi 6 MIMO Wireless LAN + Bluetooth 5.1 Combo LGA Module
Major Chipset	NXP IW620P
Host Interface	WiFi + BT ● PCIe2.0 + UART
Dimension	22 mm X 30 mm x 3.65 mm(Max) (Tolerance remarked in mechanical drawing)
Form factor	M.2 2230 Key E
Antenna	2T2R for WiFi, standalone antenna for BT ANT1(BT): BT ANT2(Aux)：WiFi_B→ TX/RX ANT3(Main)：WiFi_A → TX/RX
Weight	4g

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11 a/b/g/n/ac/ax 2T2R
WLAN VID/PID	TBD
WLAN SVID/SPID	TBD
Frequency Rage	2.4 GHz ISM Bands 2.412-2.472 GHz 5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe 5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe 5.47-5.725 GHz for Europe 5.725-5.825 GHz (FCC UNII-high band) for US/Canada
Modulation	DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM, 256QAM, 1024QAM, OFDMA
Number of Channels	2.4GHz: ■ USA, NORTH AMERICA, Canada and Taiwan - 1 ~ 11 ■ China, Australia, Most European Countries - 1 ~ 13 ■ Japan, 1 ~ 13 5GHz: ■ USA, Canada, Most European Countries -

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<table>
<tr><td></td><td>36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140,149,153,157,161,165
■ Japan - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140
■ China - 36,40,44,48,52,56,60,64, 149,153,157,161,165</td></tr>
<tr><td>Output Power</td><td>2.4G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11b (11Mbps) @EVM<35%</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11g (54Mbps) @EVM≦-27 dB</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7) @EVM≦-28 dB</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7) @EVM≦-28 dB</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11n (HE20 MCS11) @EVM≦-35 dB</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11n (HE40 MCS11) @EVM≦-35 dB</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
</table>
5G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11a (54Mbps) @EVM≦-27 dB</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7) @EVM≦-28 dB</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7) @EVM≦-28 dB</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11ac(VHT20 MCS8) @EVM≦-31 dB</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11ac(VHT40 MCS9) @EVM≦-32 dB</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11ac(VHT80 MCS9) @EVM≦-32 dB</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11ax(HE20 MCS11) @EVM≦-35 dB</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11ax(HE40 MCS11) @EVM≦-35 dB</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11ax(HE80 MCS11) @EVM≦-35 dB</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
</table></td></tr>
</table>

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<table>
<tr><td>Receiver Sensitivity</td><td>
2.4G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11b (11Mbps)</td><td>-</td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11g (54Mbps)</td><td>-</td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td>-</td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11ax(HE20 MCS11)</td><td>-</td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11ax(HE40 MCS11)</td><td>-</td><td>TBD</td><td></td><td>dBm</td></tr>
</table>
5G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11a (54Mbps)</td><td>-</td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td>-</td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11ac(VHT20 MCS8)</td><td>-</td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11ac(VHT40 MCS9)</td><td>-</td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11ac(VHT80 MCS9)</td><td>-</td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11ax(HE20 MCS11)</td><td>-</td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11ax(HE40 MCS11)</td><td>-</td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11ax(HE80 MCS11)</td><td>-</td><td>TBD</td><td></td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Data Rate</td><td>■ 802.11b: 1, 2, 5.5, 11Mbps
■ 802.11a/g: 6, 9, 12, 18, 24, 36, 48, 54Mbps
■ 802.11n: up to 150Mbps-single
■ 802.11n: up to 300Mbps-2x2 MIMO
■ 802.11ac:up to 192.6Mbps (20MHz channel)
■ 802.11ac:up to 400Mbps (40MHz channel)
■ 802.11ac:up to 866.7Mbps (80MHz channel)
■ 802.11ax:2.4GHz up to 458Mbps, 5GHz up to 1.2Gbps</td></tr>
<tr><td>Security</td><td>WiFi: WPA/WPA3</td></tr>
</table>

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Bluetooth

Features	Description
Bluetooth Standard	Bluetooth 5.1
Bluetooth VID/PID	N/A
Frequency Rage	2402MHz~2483MHz
Modulation	Header GFSK Payload 2M: π/4-DQPSK Payload 3M: 8DPSK

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Output Power		Min	Typ	Max	Unit
	BDR		2		dBm
	EDR		0		dBm
	Low Energy (2MHz)		2		dBm
Receiver Sensitivity		Min	Typ	Max	Unit
	BDR		TBD		dBm
	EDR		TBD		dBm
	Low Energy (2MHz)		TBD		dBm

1.3.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	3.3V+-5%
Operating Temperature	-10 ℃~ 85℃
Operating Humidity	less than 85% R.H.
Storage Temperature	-40 ℃~ 85℃
Storage Humidity	less than 60% R.H.

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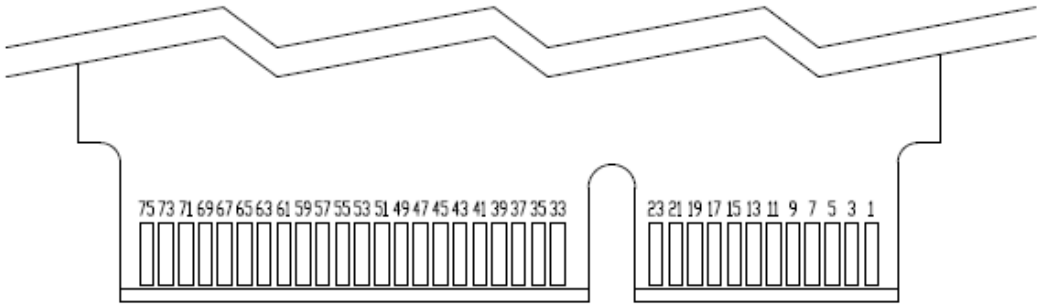
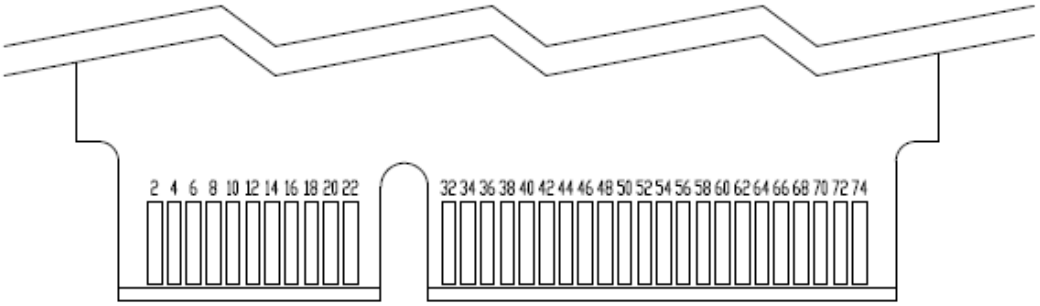
2. Pin Definition

2.1 Pin Map



PIN DEFINED (TOP VIEW)



PIN DEFINED (BOTTOM VIEW)

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2.2 Pin Table

Pin No.	Definition	Basic Description	Voltage	Type
1	GND	Ground.		GND
2	VDD33	3.3V power supply	3.3V	VCC
3	NC	NC		Floating
4	VDD33	3.3V power supply	3.3V	VCC
5	NC	NC		Floating
6	NC	NC		Floating
7	GND	Ground.		GND
8	PCM_CLK	PCM mode: PCM_CLK	1.8V	I/O
9	NC	NC		Floating
10	PCM_SYNC	PCM mode: PCM_SYNC	1.8V	I/O
11	NC	NC		Floating
12	PCM_OUT	PCM mode: PCM_OUT	1.8V	O
13	NC	NC		Floating
14	PCM_IN	PCM mode: PCM_IN	1.8V	I
15	NC	NC		Floating
16	NC	NC		Floating
17	NC	NC		Floating
18	GND	Ground.		GND
19	NC	NC		Floating
20	UART_WAKE	UART WAKE/GPIO14	3.3V	I
21	NC	NC		Floating

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22	UART_TX	UART SOUT pin	1.8V	O
23	NC	NC		Floating
32	UART_RX	UART SIN.pin	1.8V	I
33	GND	Ground.		GND
34	UART_RTSn	UART Mode: UART_RTSn (active low)	1.8V	O
35	PERp0	PCIe Differential receive.	1.8V	I
36	UART_CTSn	UART Mode: UART_CTSn (active low)	1.8V	I
37	PERn0	PCIe Differential receive.	1.8V	I
38	TDO	TDO/GPIO21	1.8V	I/O
39	GND	Ground.		GND
40	GPIO12	GPIO12	1.8V	I/O
41	PETp0	PCIe Differential transmit.	1.8V	O
40	GPIO13	GPIO13	1.8V	I/O
43	PETn0	PCIe Differential transmit.	1.8V	O
44	TDI	TDI/GPIO20	1.8V	I/O
45	GND	Ground.		GND
46	TCK	TCK/GPIO18	1.8V	I/O
47	REFCLKP	PCIe Differential reference clock.	1.8V	I
48	TMS	TMS/GPIO19	1.8V	I/O
49	REFCLKN	PCIe Differential reference clock.	1.8V	I
50	NC	NC		Floating
51	GND	Ground.		GND
52	PERST0	PCI Express Reset Signal: active low.	3.3V	I

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53	CLKREQ0	Reference clock request	3.3V	O
54	W_DISABLE2#	W_DISABLE2#/GPIO15	3.3V	I
55	PEWAKE#	Open Drain active Low signal.	3.3V	O
56	PDn	Full power down for WLAN/BT	3.3V	I
57	GND	Ground.		GND
58	NC	NC		Floating
59	NC	NC		Floating
60	NC	NC		Floating
61	NC	NC		Floating
62	NC	NC		Floating
63	GND	Ground.		GND
64	NC	NC		Floating
65	NC	NC		Floating
66	NC	NC		Floating
67	NC	NC		Floating
68	NC	NC		Floating
69	GND	Ground.		GND
70	NC	NC		Floating
71	NC	NC		Floating
72	VDD33	3.3V power supply	3.3V	VCC
73	NC	NC		Floating
74	VDD33	3.3V power supply	3.3V	VCC
75	GND	Ground		GND

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3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
3V3	DC supply for the 3.3V input	-	3.3	3.63	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
3.3V	DC supply for the 3.3V input	3.14	3.3	3.46	V

3.3 Digital IO Pin DC Characteristics

3.3.1 3.3V Operation (VIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO	-	VIO+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3*VIO	
V_{OH}	Output High Voltage	VIO-0.4	-	-	
V_{OL}	Output Low Voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

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3.4 Host Interface

3.4.1 PCI Express Interface

3.4.1.1 Differential Tx Output Electricals – 2.5GT/s

symbol	parameter	Min	Typ	Max	Units
UI	Unit interval (UI) The specified UI is equivalent to a tolerance of ±300 ppmfor each Refclk source. Period does not account for SSC induced variations.	399.88	-	400.12	ps
$V_{Tx-DIFF-PP}$	Differential peak-to-peak Tx voltage swing $V_{Tx-DIFFpp} = 2*\|V_{TXD+} - V_{TXD-}$	0.8	-	1.2	V
$V_{Tx-DIFF-PP-LOW}$	Low power differential peak-to-peak Tx voltage swing $V_{Tx-DIFFpp} = 2*\|V_{TXD+} - V_{TXD-}\|$	0.4	-	1.2	V
$V_{Tx-DE-RATIO-3.5dB}$	Tx de-emphasis level ratio (3.5 dB)	3.0	-	4.0	dB
T_{Tx-EYE}	Tx eye including all jitter sources	0.75	-	-	UI
$T_{Tx-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between jitter median and maximum deviation from median	-	-	0.125	UI
$T_{Tx-RISE-FALL}$	Tx rise/fall time Measured differentially from 20% to 80% of swing.	0.125	-	-	UI
$RL_{Tx-DIFF}$	Tx package plus Si differential return loss	10	-	-	dB
RL_{Tx-CM}	Tx package plus Si common mode return loss	6	-	-	dB
$V_{Tx-CM-AC-P}$	Tx AC common mode voltage	-	20	-	mV
$I_{Tx-SHORT}$	Tx short circuit current limit	-	-	90	mA
$V_{Tx-DC-CM}$	Tx DC common mode voltage	0	-	3.6	V
$V_{Tx-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle	0	-	100	mV
$V_{Tx-IDLE-DIFF-AC-p}$	Electrical idle differential peak output voltage	0	-	20	mV
$V_{Tx-RCV-DETECT}$	Voltage change allowed during receiver detection	-	-	600	mV
$T_{Tx-IDLE-MIN}$	Minimum time spent in electrical idle	20	-	-	ns
$T_{Tx-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	-	-	8	ns
$T_{Tx-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid diff signaling after leaving electrical idle	-	-	8	ns
$T_{CROSSLINK}$	Crosslink random timeout	-	-	1.0	ms
C_{Tx}	AC coupling capacitor	75	-	200	nF

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3.4.1.2 Differential Tx Output Electricals – 5GT/s

symbol	parameter	Min	Typ	Max	Units
UI	Unit interval (UI) The specified UI is equivalent to a tolerance of ±300 ppmfor each Refclk source. Period does not account for SSC induced variations.	199.94	-	200.06	ps
$V_{Tx-DIFF-PP}$	Differential peak-to-peak Tx voltage swing $V_{Tx-DIFFpp} = 2*\|V_{TXD+} - V_{TXD-}$	0.8	-	1.2	V
$V_{Tx-DIFF-PP-LOW}$	Low power differential peak-to-peak Tx voltage swing $V_{Tx-DIFFpp} = 2*\|V_{TXD+} - V_{TXD-}\|$	0.4	-	1.2	V
$V_{Tx-DE-RATIO-3.5dB}$	Tx de-emphasis level ratio (3.5 dB)	3.0	-	4.0	dB
$V_{Tx-DE-RATIO-3.5dB}$	Tx de-emphasis level ratio (6 dB)	5.5	-	6.5	dB
$T_{Min-PULSE}$	Instantaneous lone pulse width Measured relative to rising/falling pulse	0.9	-	-	UI
T_{Tx-EYE}	Tx eye including all jitter sources	0.75	-	-	UI
$T_{Tx-HF-DJ-DD}$	Tx deterministic jitter > 1.5 MHz Deterministic jitter only	-	-	0.15	UI
$T_{Tx-LF-RMS}$	Tx RMS jitter < 1.5 MHz Total energy measured over a 10kHz~1.5 MHz range.	-	3.0	-	ps RMS
$T_{Tx-RISE-FALL}$	Tx rise/fall time Measured differentially from 20% to 80% of swing.	0.15	-	-	UI
$RL_{Tx-DIFF}$	Tx package plus Si differential return loss(0.05~1.25 GHz)	10	-	-	dB
	Tx package plus Si differential return loss(1.25~2.5 GHz)	8	-	-	
RL_{Tx-CM}	Tx package plus Si common mode return loss	6	-	-	dB
$V_{Tx-CM-AC-P}$	Tx AC common mode voltage	-	-	100	mVPP
$I_{Tx-SHORT}$	Tx short circuit current limit	-	-	90	mA
$V_{Tx-DC-CM}$	Tx DC common mode voltage	0	-	3.6	V
$V_{Tx-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle	0	-	100	mV
$V_{Tx-IDLE-DIFF-AC-p}$	Electrical idle differential peak output voltage $V_{Tx-IDLE-DIFF-DC} = \|V_{Tx-Idle-D+} - V_{Tx-Idle-D-}\| \leq 20$ mV	0	-	20	mV
$V_{Tx-IDLE-DIFF-DC}$	DC electrical idle differential output voltage $V_{Tx-IDLE-DIFF-DC} = \|V_{Tx-Idle-D+} - V_{Tx-Idle-D-}\| \leq 5$ mV	0	-	5	mV
$V_{Tx-RCV-DETECT}$	Voltage change allowed during receiver detection	-	-	600	mV
$T_{Tx-IDLE-MIN}$	Minimum time spent in electrical idle	20	-	-	ns
$T_{Tx-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	-	-	8	ns
$T_{Tx-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid diff signaling after leaving electrical idle	-	-	8	ns
$T_{CROSSLINK}$	Crosslink random timeout	-	-	1.0	ms
C_{Tx}	AC coupling capacitor	75	-	200	nF

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3.4.1.3 Differential Rx Input Electricals – 2.5GT/s

symbol	parameter	Min	Typ	Max	Units
UI	Unit Interval (UI) UI does not account for SSC induced variations.	399.88	-	400.12	ps
$V_{Rx-DIFF-PP-CC}$	Differential Rx peak-to-peak voltage for common Refclk Rx architecture-	0.175	-	1.2	V
$V_{Rx-DIFF-PP-DC}$	Differential Rx peak-to-peak voltage for data clocked Rx architecture	0.175	-	1.2	V
T_{Rx-EYE}	Rx eye time opening Minimum eye time at Rx pins to yield a 10^{-12} BER	0.4	-	-	UI
$T_{Rx-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between jitter median and maximum deviation from median	-	-	0.3	UI
$V_{Rx-CM-ACp}$	AC peak common mode voltage	-	-	150	mV
$RL_{Rx-DIFF}$	Differential return loss	15	-	-	dB
RL_{Rx-CM}	common mode return loss	-	-	3.6	dB
$Z_{Rx-DIFF-DC}$	DC differential input impedance	80	100	120	Ω
Z_{Rx-DC}	DC input impedance	40	50	60	Ω
$Z_{Rx-HIGH-IMP-DC}$	Powered down DC input impedance	200	-	-	kΩ
$V_{Rx-IDLE-DET-DIFF-p-p}$	Electrical idle detect threshold	65	-	175	mV
$T_{Rx-IDLE- DET-DIFF-ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time	-	-	10	ms
$L_{Rx-SKEW}$	Total skew	-	-	20	ns

3.4.1.4 Differential Rx Input Electricals – 5GT/s

symbol	parameter	Min	Typ	Max	Units
UI	Unit Interval (UI) UI does not account for SSC induced variations.	199.44	-	200.06	ps
$V_{Rx-DIFF-PP-CC}$	Differential Rx peak-to-peak voltage for common Refclk Rx architecture-	0.12	-	1.2	V
$V_{Rx-DIFF-PP-DC}$	Differential Rx peak-to-peak voltage for data clocked Rx architecture	0.1	-	1.2	V
$T_{Rx-TJ-CC}$	Maximum Rx inherent total timing error for common Refclk Rx architecture	-	-	0.4	UI
$T_{Rx-TJ-DC}$	Maximum Rx inherent total timing error for data clocked Rx architecture	-	-	0.34	UI
$T_{Rx-DJ-DD-CC}$	Maximum Rx inherent deterministic timing error for common Refclk Rx architecture	-	-	0.3	UI
$T_{Rx-DJ-DD-DC}$	Maximum Rx inherent deterministic timing error for data clocked Rx architecture	-	-	0.24	UI

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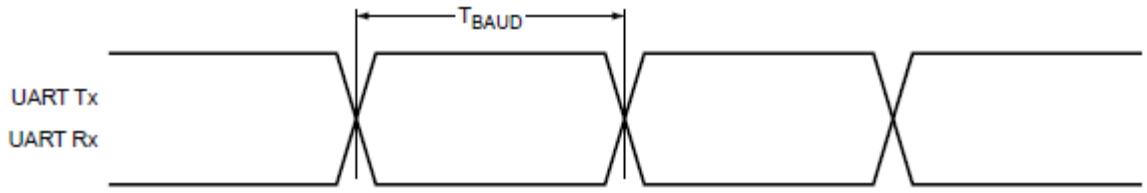
$T_{Rx\text{-}MIN\text{-}PULSE}$	Minimum width pulse at Rx Measured to account for worst Tj at 10^{-12} BER.	0.6	-	-	UI
$V_{Rx\text{-}CM\text{-}ACp}$	AC peak common mode voltage	-	-	150	mV
$RL_{Rx\text{-}DIFF}$	Differential return loss	15	-	-	dB
$RL_{Rx\text{-}CM}$	common mode return loss	-	-	3.6	dB
$Z_{Rx\text{-}DIFF\text{-}DC}$	DC differential input impedance	80	100	120	Ω
$Z_{Rx\text{-}DC}$	DC input impedance	40	50	60	Ω
$Z_{Rx\text{-}HIGH\text{-}IMP\text{-}DC}$	Powered down DC input impedance	200	-	-	kΩ
$V_{Rx\text{-}IDLE\text{-}DET\text{-}DIFF\text{-}p\text{-}p}$	Electrical idle detect threshold	65	-	175	mV
$T_{Rx\text{-}IDLE\text{-}DET\text{-}DIFF\text{-}ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time	-	-	10	ms
$L_{Rx\text{-}SKEW}$	Total skew	-	-	20	ns

3.4.2.High-Speed UART Interface

The AW-XM455MA supports a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface, compliant to the industry standard 16550 specification. High-speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data.



Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{BAUD}	Baud rate	26MHz input clock	250	-	-	ns

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3.5 Timing Sequence

AW-XM455MA power up timing sequence.

TBD

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3.6 Power Consumption*

3.6.1 WLAN

TBD

3.6.2 Bluetooth

TBD

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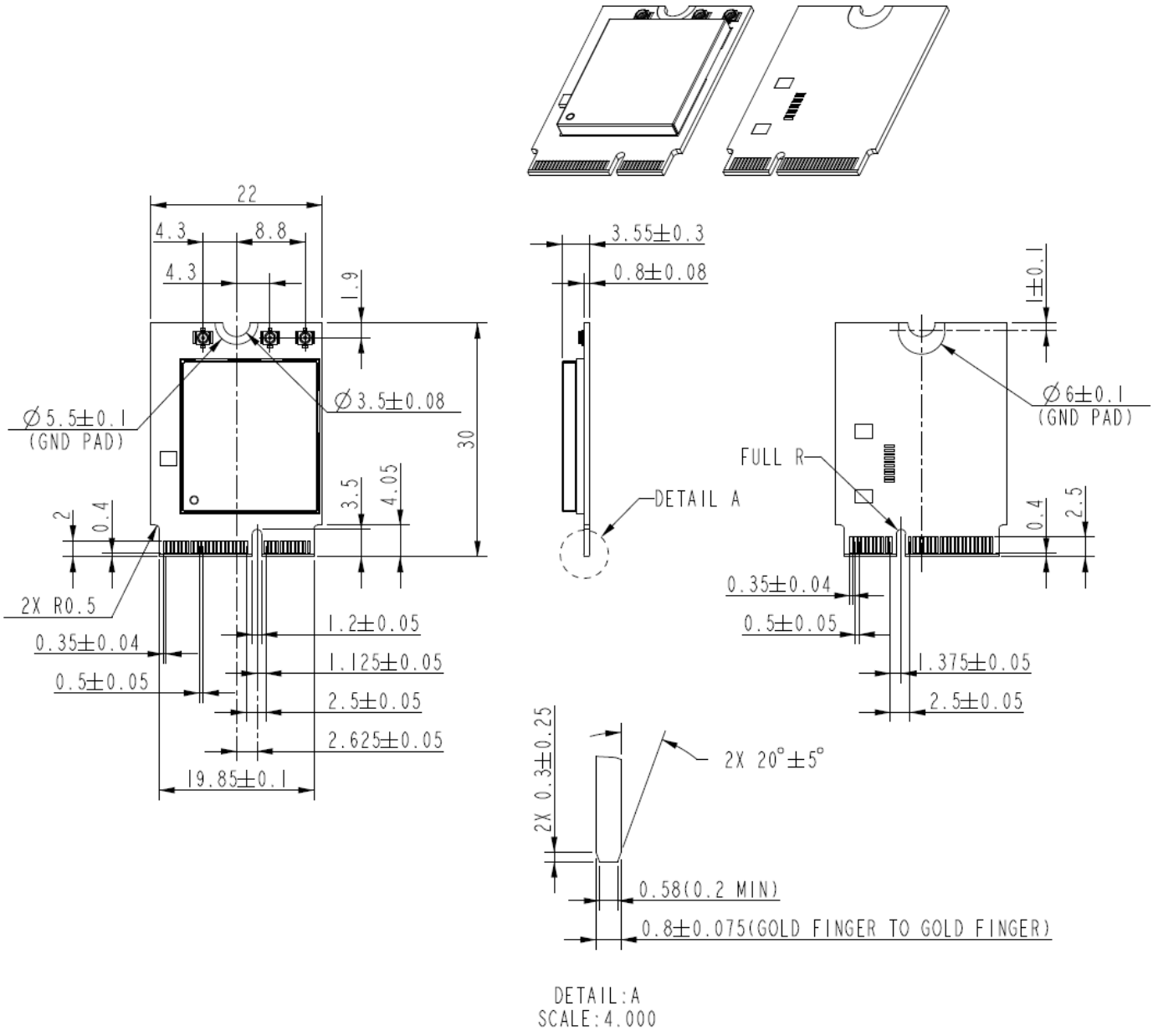
4. Mechanical Information

4.1 Mechanical Drawing



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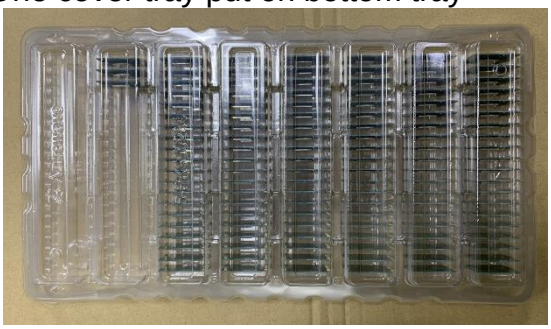
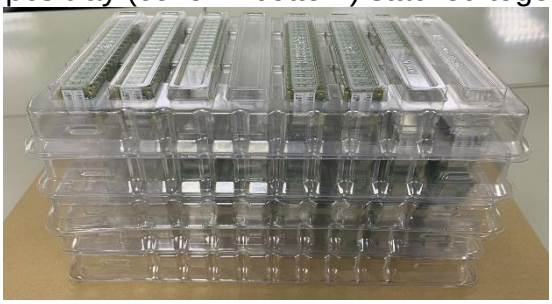
5. Packing Information

1. 160pcs M.2 2230 modules put in the one bottom tray

2. One cover tray put on bottom tray



3. 5pcs tray (cover + bottom) stacked together



4. Use P.P Strap to pack 5 trays

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5. Put packed trays into inner box

6. Seal the inner box by AzureWave tape

7. One package label pasted in side of inner box

Example:

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8. Two inner boxes put into one carton; If only one inner box has modules, “Empty” label pasted on the other one inner box

Example:

9. Seal the carton by AzureWave tape

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10. One carton label and box label pasted on the carton. If the carton is not full, one balance label pasted on the carton

Example of carton label	AzureWave P/N: Customer: 由業務提供 Customer P/N: 由業務提供 Customer PO: 由業務提供 Description: AW-XXXXXX QTY: 1200 pcs C/N: N.W. / G.W. RoHS COMPLIANT
Example of box label	
Example of production label	
Example of balance label	

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